ASML

EUV Lithography for cost effective extension of Moore's law

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Eleven NXE:3300B systems in various states of integration

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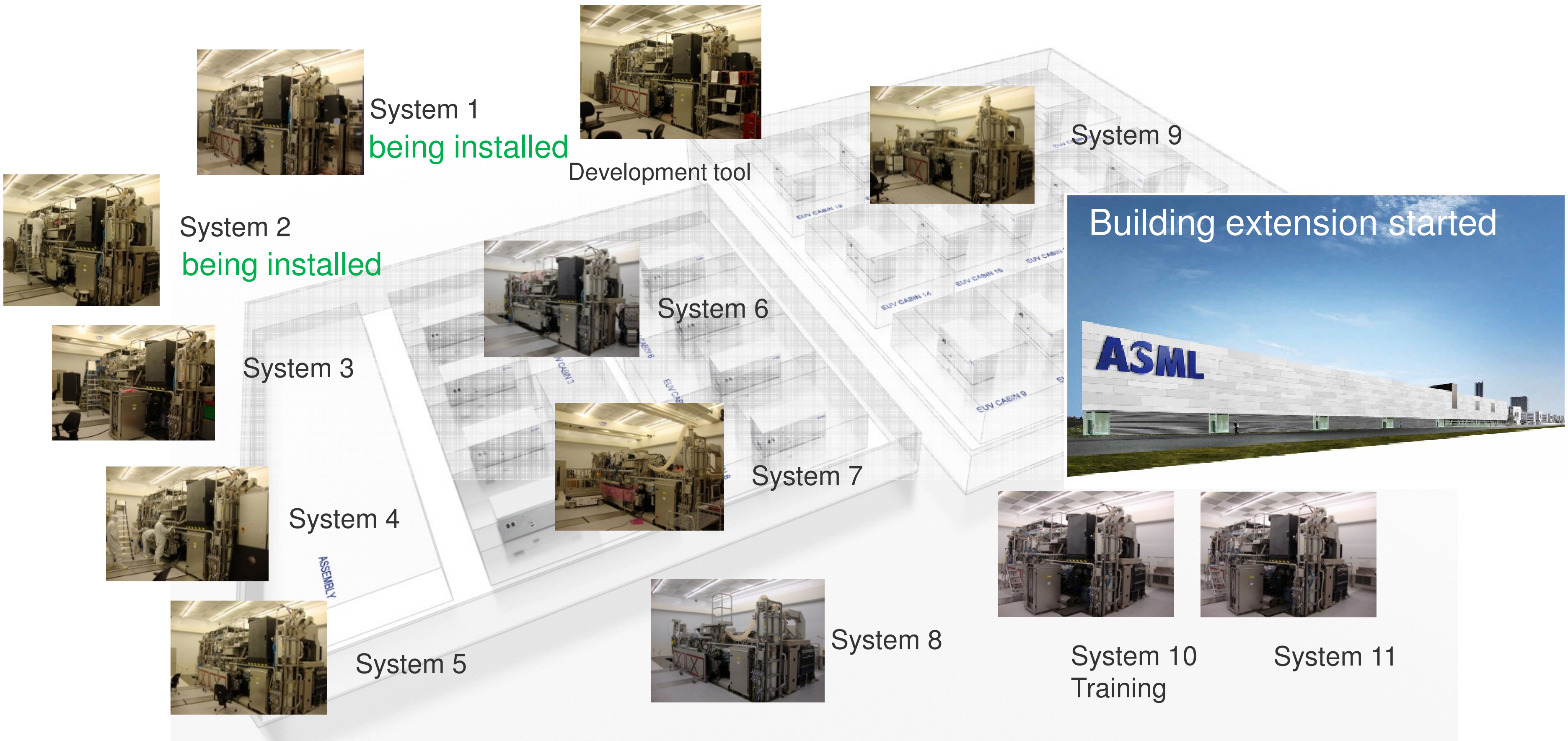


Presentation Outline

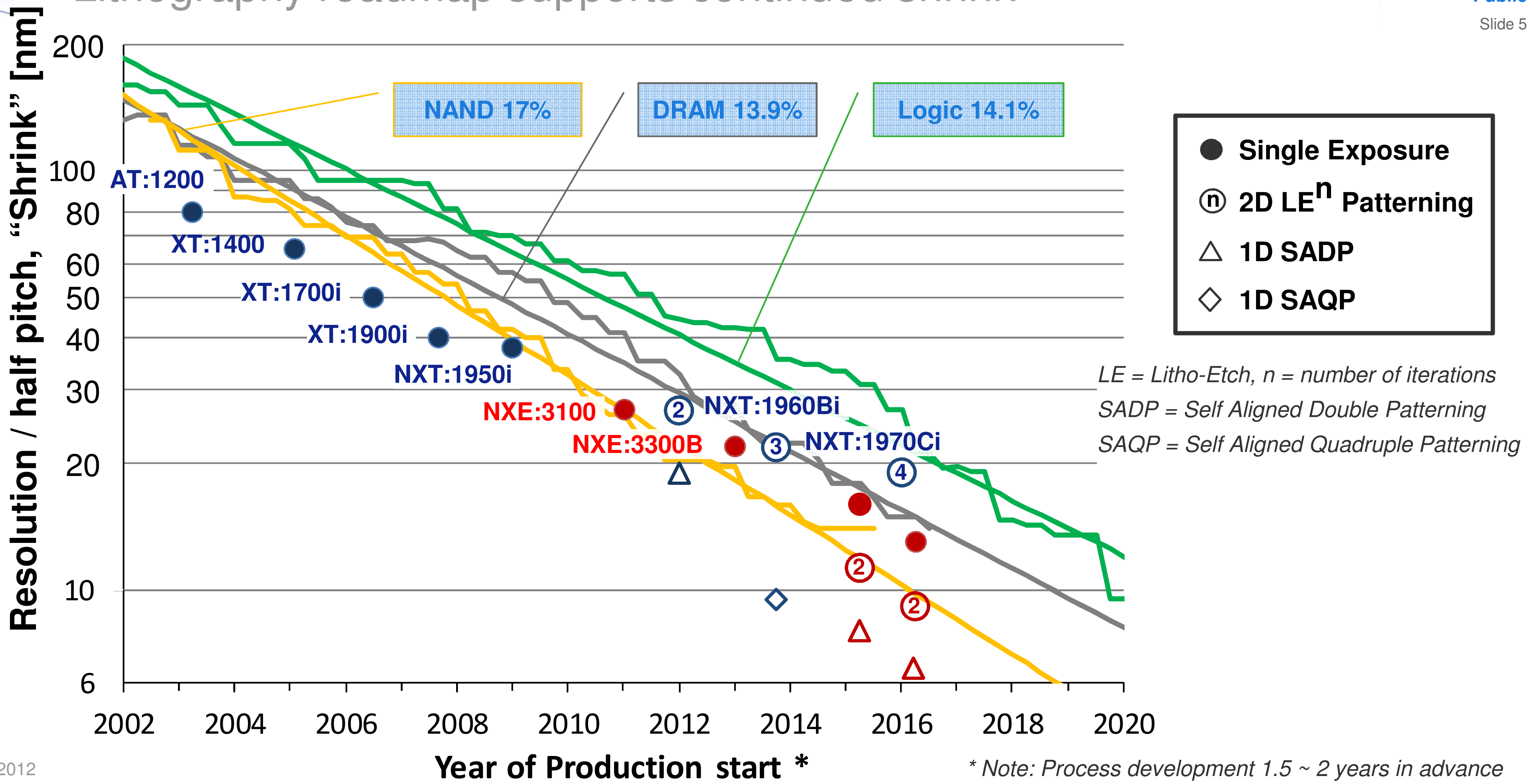
- Why EUV
- EUV status
- EUV challenge

Presentation Outline

- **Why EUV**
    - Lower cost
    - Shorter cycle times
    - Higher Fab capacity
    - Continued scaling
    - Improved electrical performance
- EUV roadmap, scanner & source status
- EUV challenges

Industry roadmap towards < 10 nm resolution

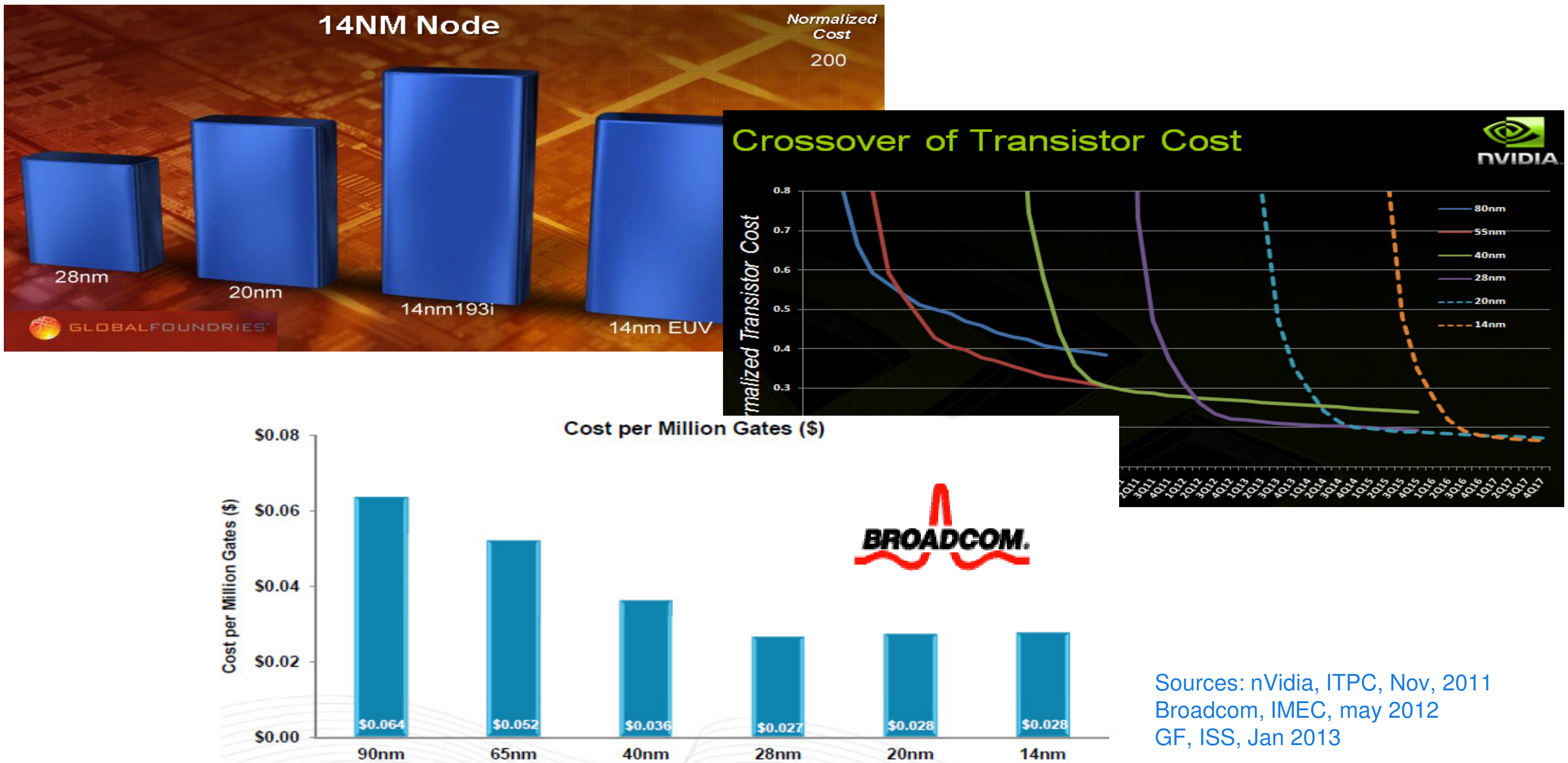
Lithography roadmap supports continued shrink



LE = Litho-Etch, n = number of iterations
SADP = Self Aligned Double Patterning
SAQP = Self Aligned Quadruple Patterning

* Note: Process development 1.5 ~ 2 years in advance

Cost scaling becomes greater concern with shrinks below 28nm



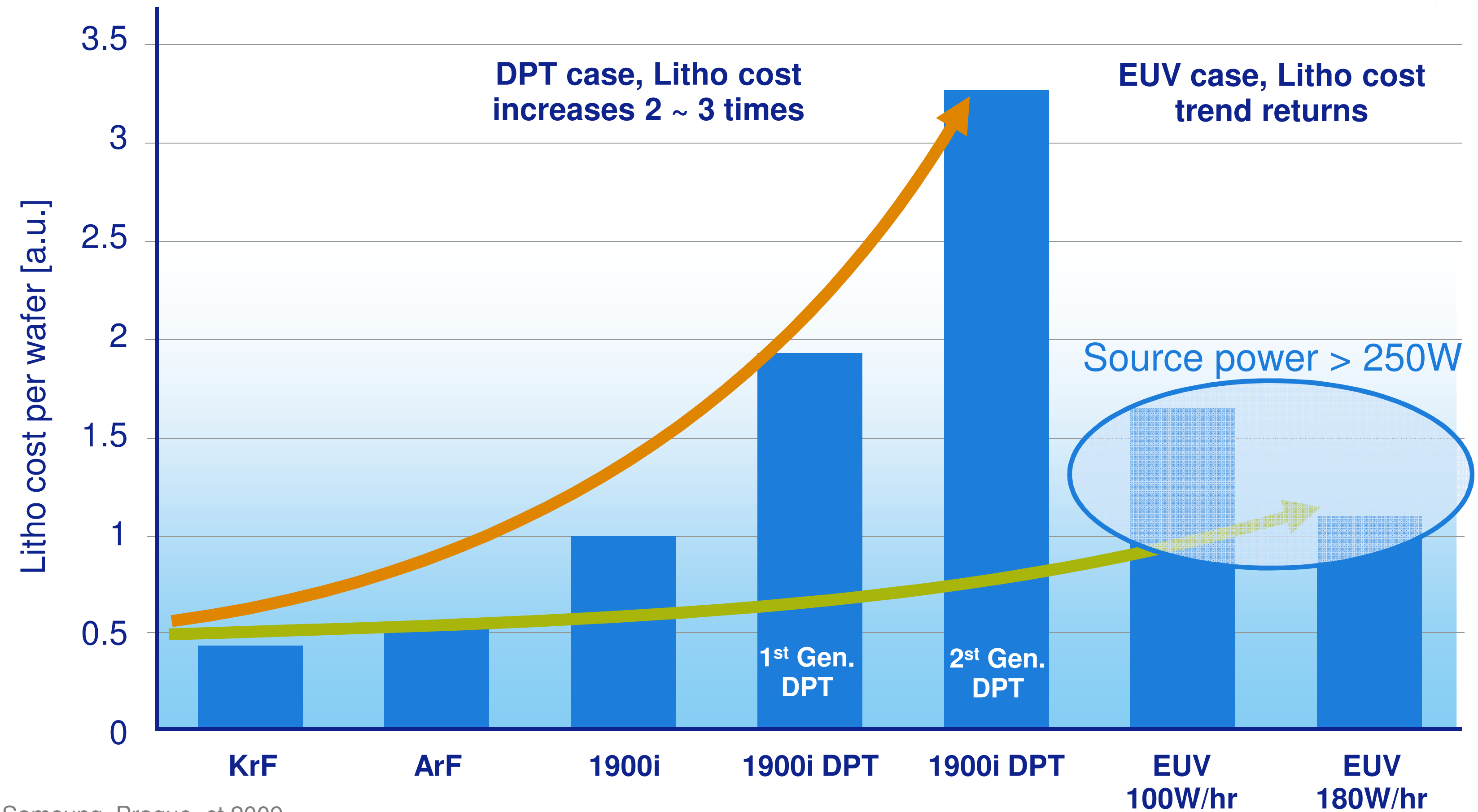
Sources: nVidia, ITPC, Nov, 2011
Broadcom, IMEC, may 2012
GF, ISS, Jan 2013

EUV reduces <u>Cost</u> and <u>Cycle Time</u> vs. Multiple Patterning

Relative to EUV	LE²	SADP	SAQP
Process Steps	x2	x4	x5
Process Cost	+10%	+30~50%	+>50%
Cycle Time	x2	x4	x5

LE = Litho-Etch, n = number of iterations
SADP = Self Aligned Double Patterning
SAQP = Self Aligned Quadruple Patterning

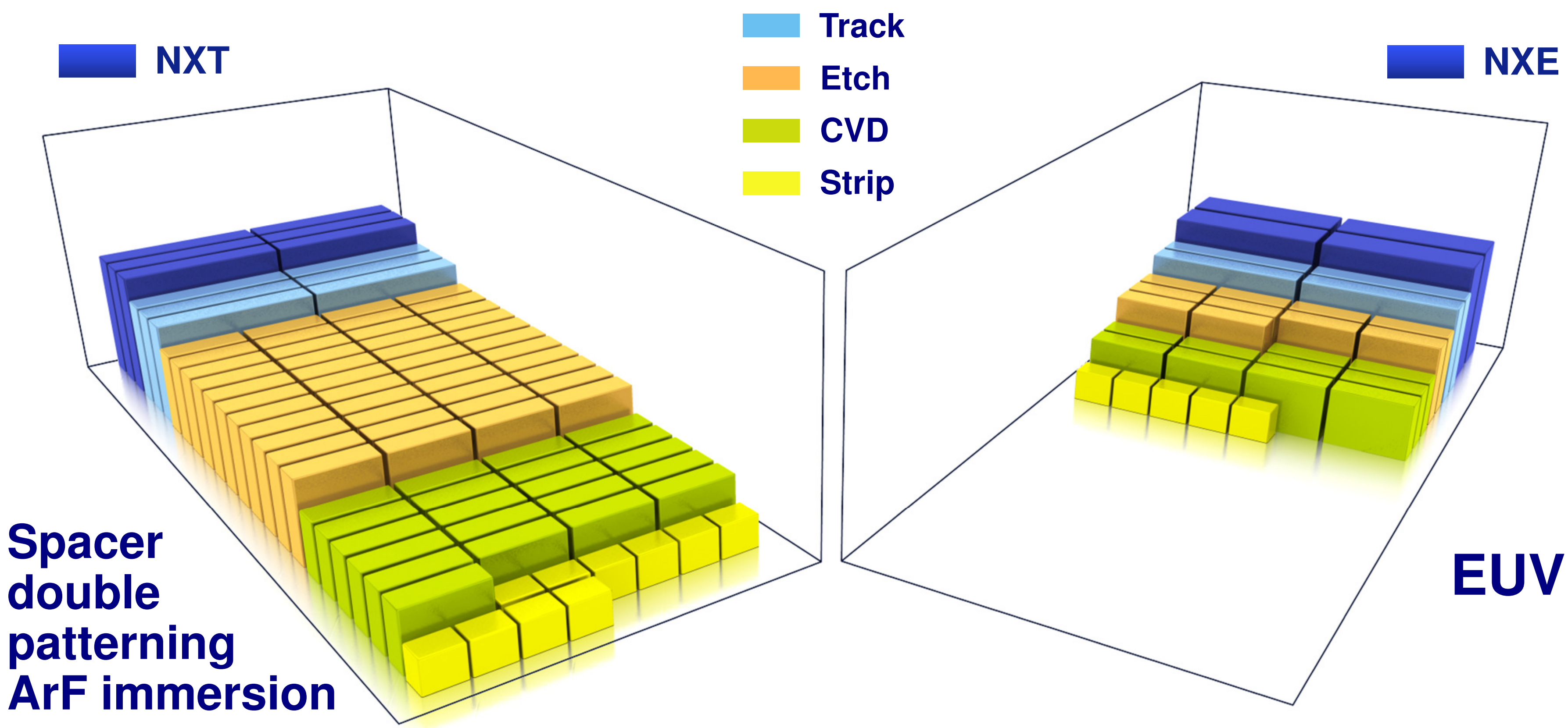
Litho Cost back to normal trend with EUV > ~70 W/hr



Source Samsung, Prague, ct 2009

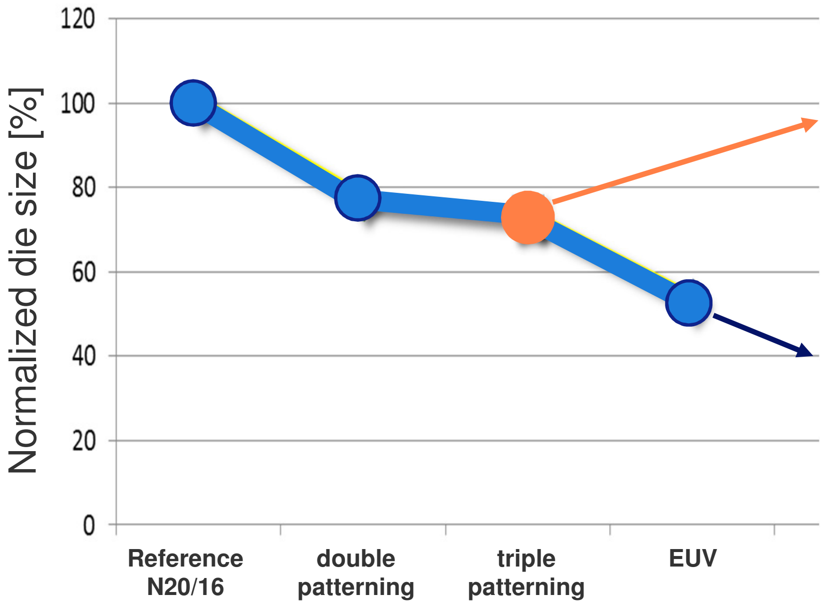
EUV increases Fab capacity for Litho ~2x

Larger footprint required to support Multi Patterning schemes

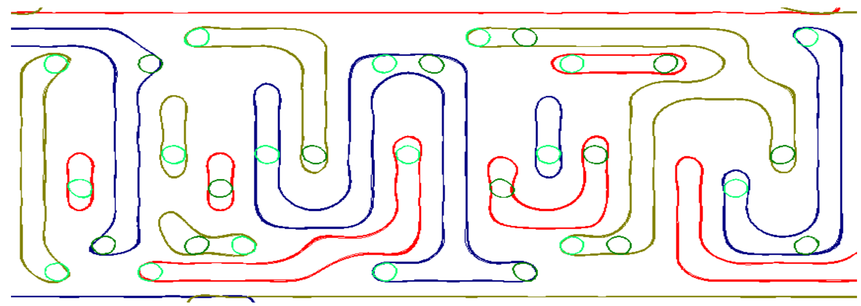


Only EUV enables 50% Scaling for the 10 nm node

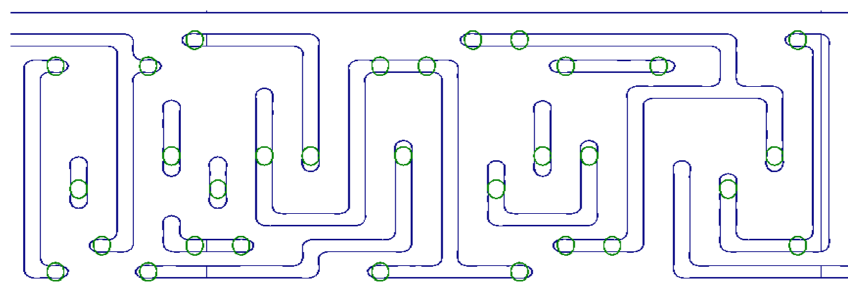
Layout restrictions and litho performance limit shrink to ~25% using immersion



Source: ARM, Scaled 20nm flip-flop design

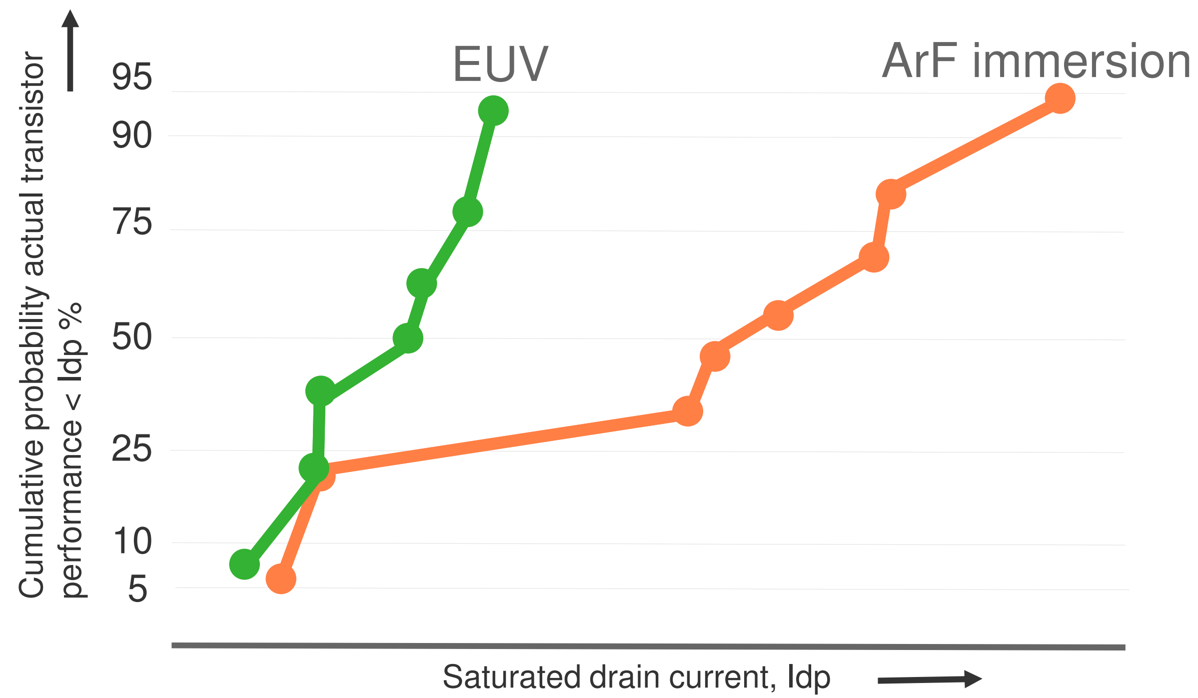


Triple patterning does not show a process window



EUV meets all litho requirements

EUV Electrical Performance distribution tighter



Source: Sam Sivakumar, Intel, SPIE, Feb 2013

Presentation Outline

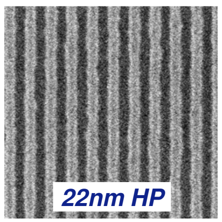
- Why EUV
- **EUV status**
  - Scanner
  - Source

EUV challenges

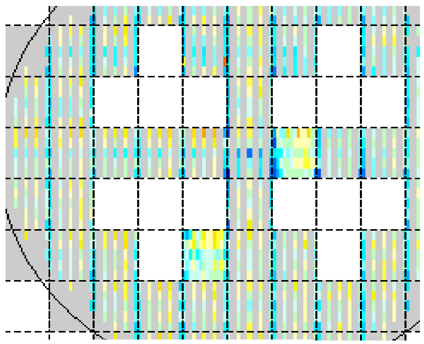
NXE:3300B imaging and overlay beyond expectations

matched overlay to immersion ~3.5nm

Scanner qualification

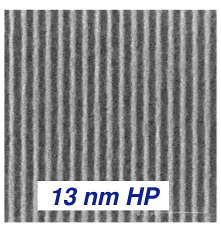


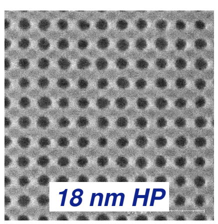
BE = 15.9 mJ/cm²
EL = 13%
DoF = 160 nm

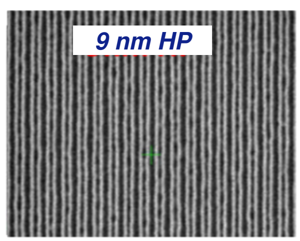


Full wafer CDU = 1.5nm

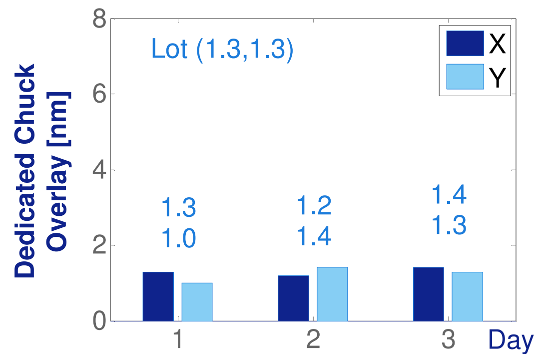
Scanner capability

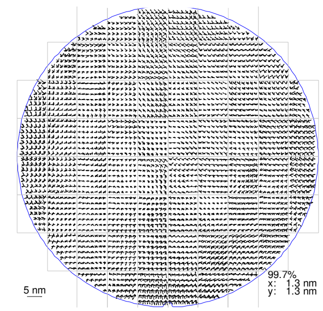


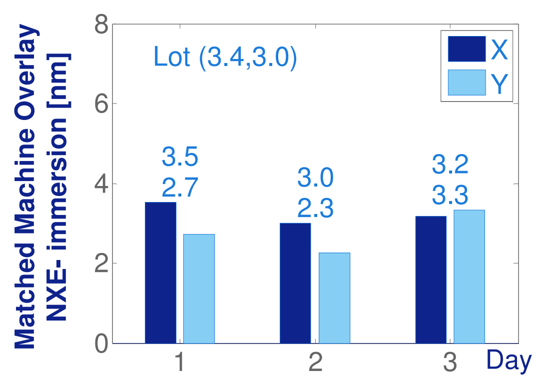


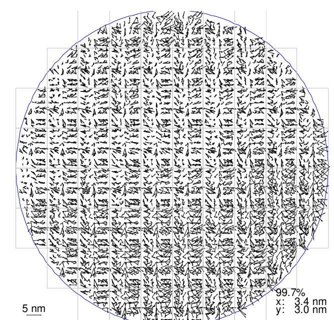


Single exposure EUV Spacer





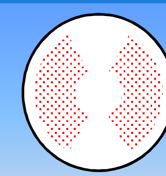




XT:1950i reference wafers
EEXY sub-recipes
18par (avg. field) +
CPE (6 par per field)

NXE technology roadmap has extendibility to <7nm

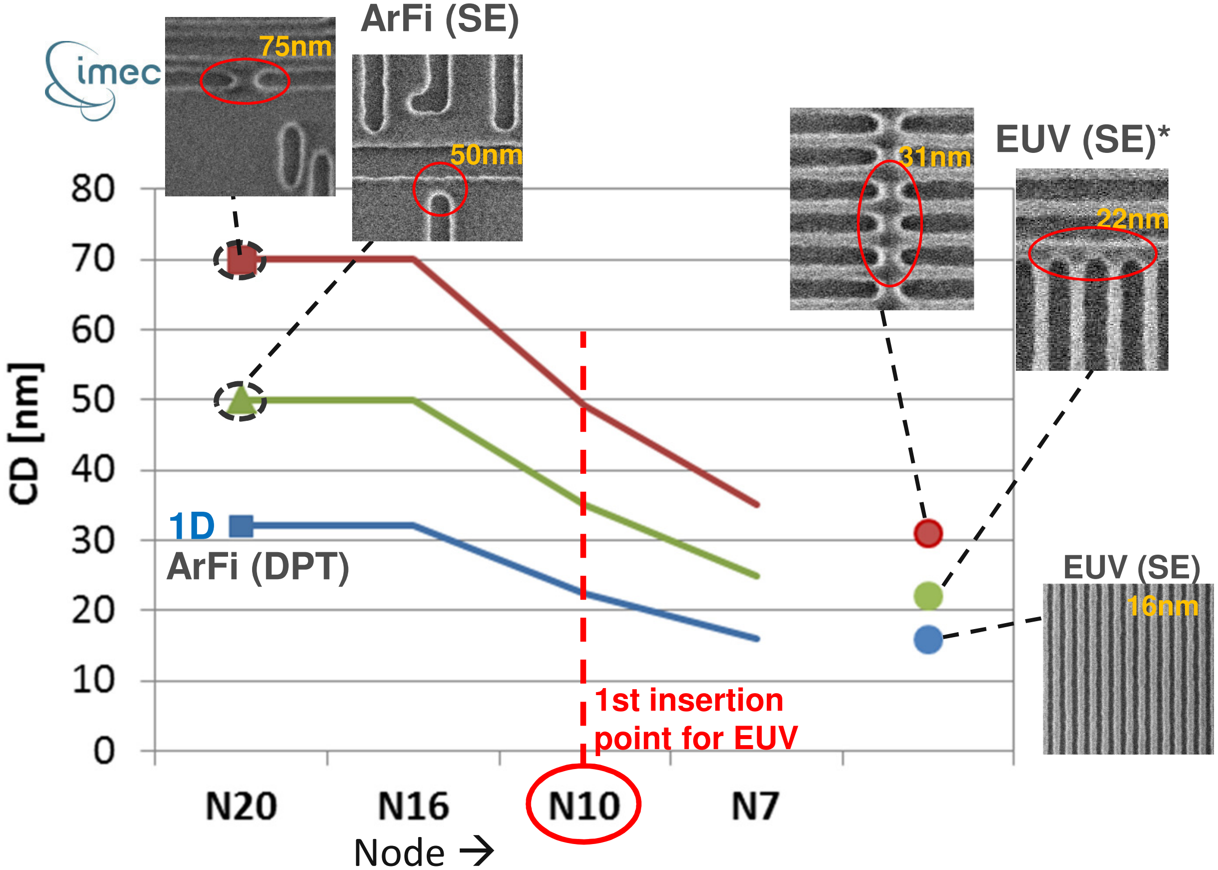
				NXE:3300B	NXE:3350B	*Under study*			
Resolution [nm]		**32**	**27**	**22**	**16**	**13**	**10**	**7**	**<7**
Wavelength [nm]		13.5							
Lens	NA	0.25		0.33			0.33NA DPT		0.45-0.60 DPT
							0.45	0.60	
	flare	8%		6%	4%				
Illumination	coherence	σ=0.5	σ=0.8	σ=0.2-0.9	FlexPupil	Extended FlexPupil			
						reduced pupil fill ratio			
Overlay	DCO [nm]	7	4.0	3.0	1.5	1.2	1.0		
	MMO [nm]	-	7.0	5.0	2.5	2.0	1.7		
TPT (300mm)	Dose [mJ/cm^2]	5	10	15	15	20	20		
	Power [W]	3	10 - 105	80 - 250	250	250	500		
	Throughput [w/hr]	-	6 - 60	50 - 125	125	125	165		

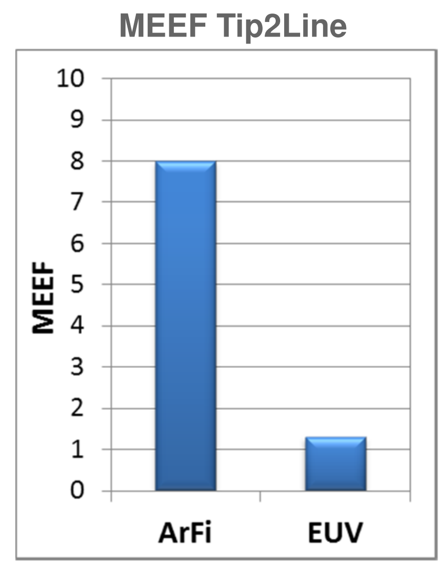


pupil fill ratio defined as the bright fraction of the pupil

EUV enables aggressive shrink on 2D logic

shrink possible beyond N7 node requirement



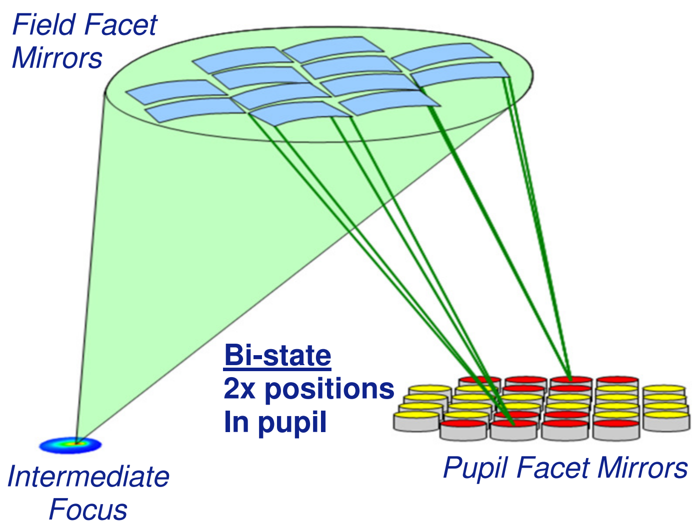


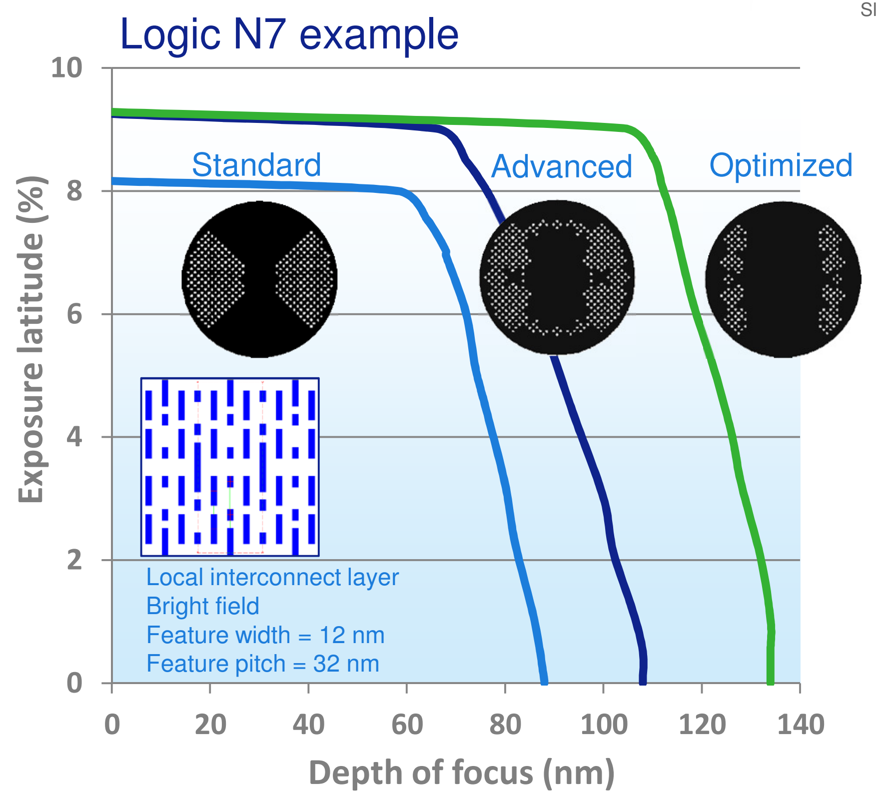
* using high dose resist @ ~50mJ

NXE:3300B FlexPupil enhances process window

Enabling further shrink at 0.33-NA

Custom pupil definition enabled by mirror addressing programmability

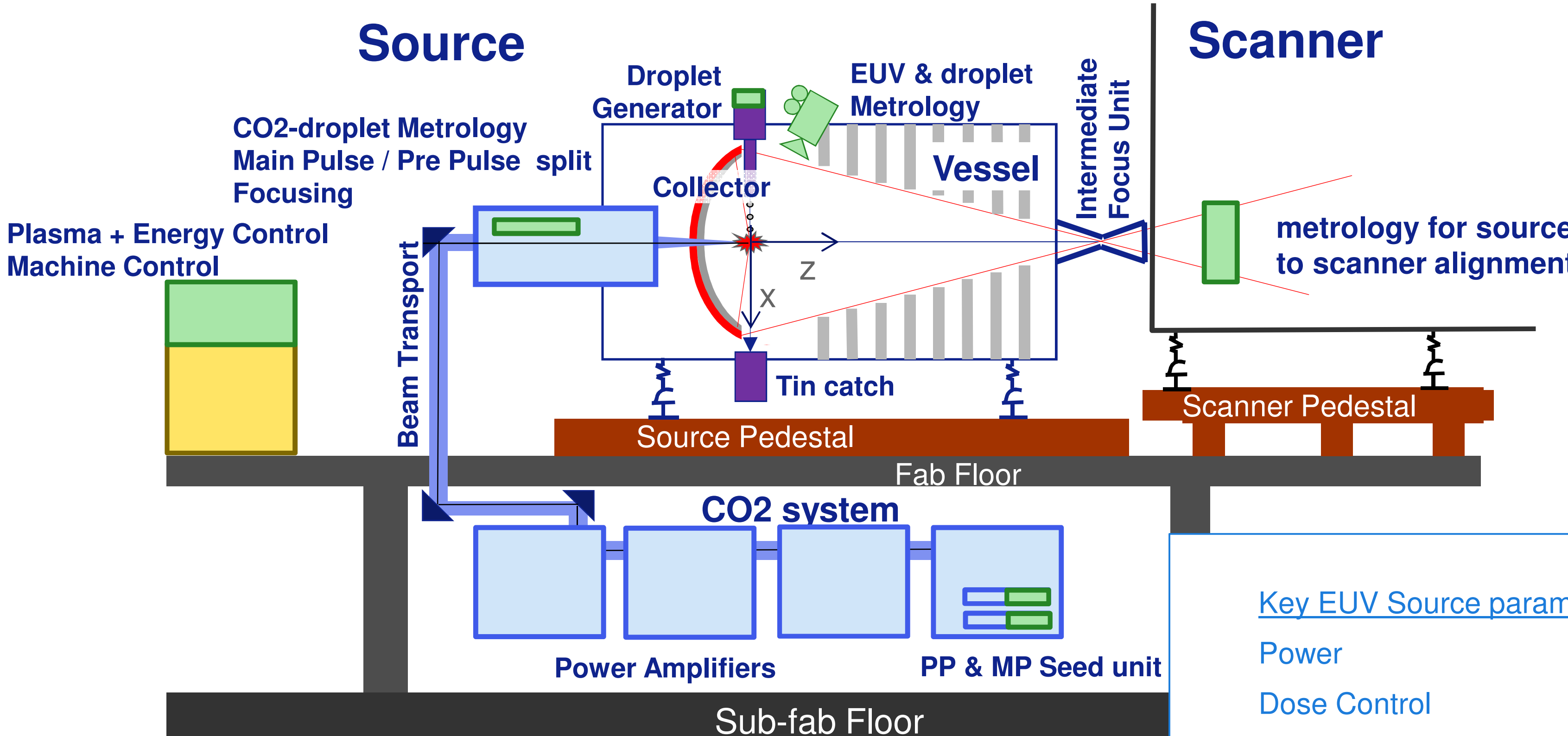




Simulations by Tachyon SMO NXE

EUV Source:

Cross-section & key performance parameters



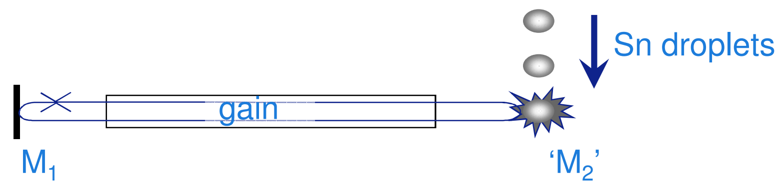
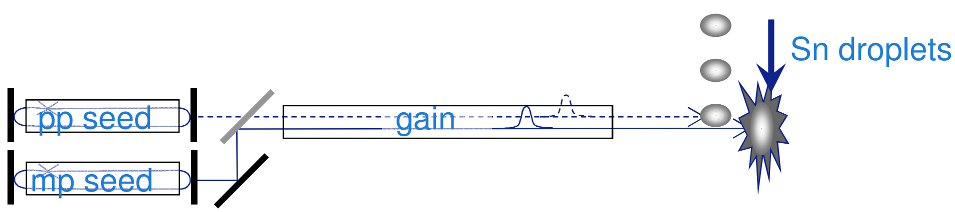
x=droplet stream direction, z=CO2 light direction, y=orthogonal

Key EUV Source parameters

- Power
- Dose Control
- Debris mitigation

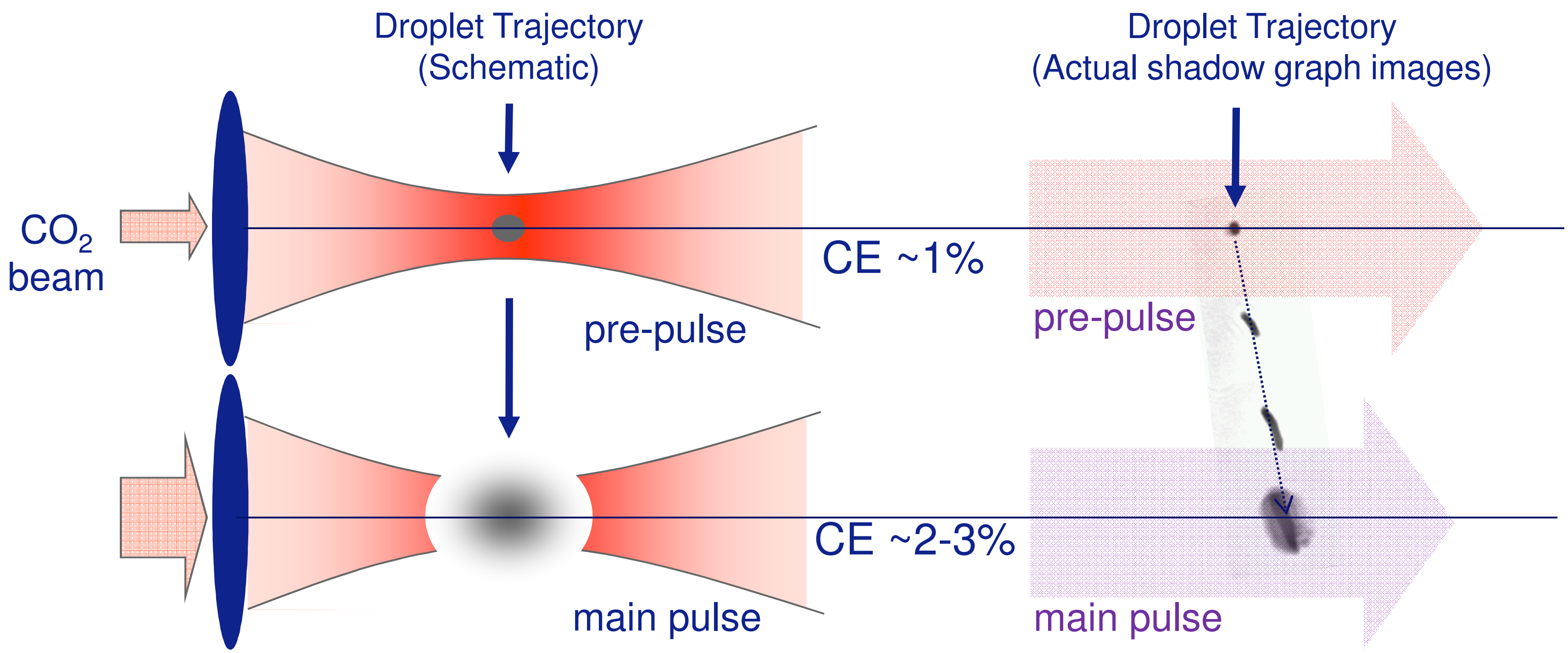
Two EUV source operating modes

- CO_2 laser pulse converts Tin (Sn) droplets into plasma emitting 13.5nm EUV
- Pre-Pulse (PP) increases Conversion Efficiency (CE) by “puffing up” the droplet

NoMo		• CE ~ 1% • Self-timed / simple • No control • Power ~ 10W
MoPA-PP		• CE ~ 3-4% • Yet more complex • Complete control • Roadmap to > 250W

Pre-Pulse – Key to scaling EUV source power

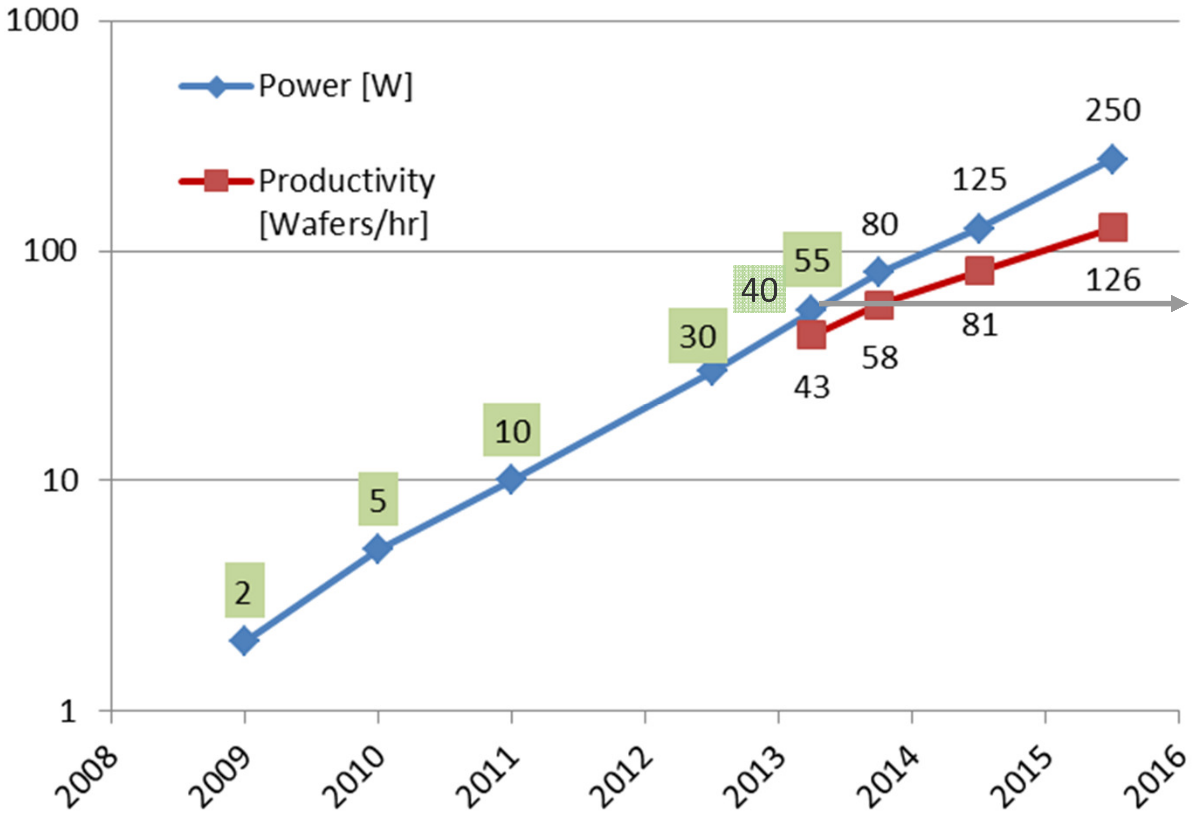
Higher Conversion Efficiency by droplet pre-puffing: MOPA+PP

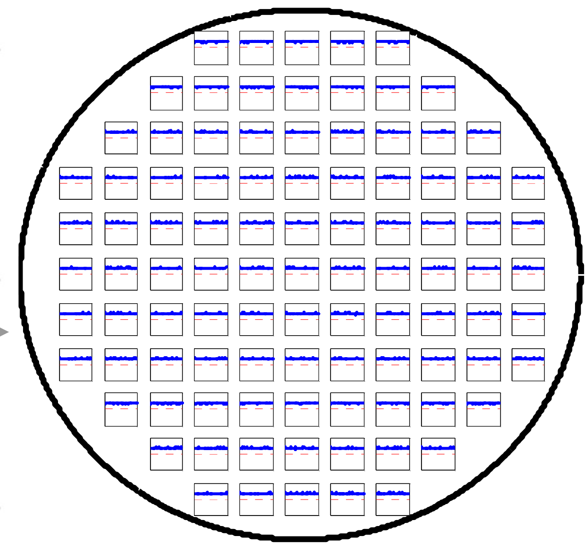


- *Droplet conditioning is required to scale EUV power*
- *Pre-puffed droplet provides better overlap with CO_2 main pulse heating beam*

EUV Source Power Progress reaching 55 W

Supporting 43 Wafers/hr; 250 W target to be reached in 2015





At 55 W, 1 run:
97.5% of the dies < 0.5% dose

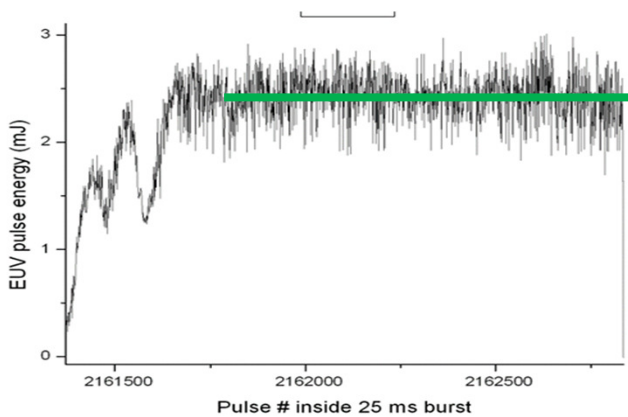
At 40 W, 6 runs:
99.99 of the dies < 0.2% dose,

7 one hour runs total representing
~ 250 exposed wafers @ 15 mJ/cm^2

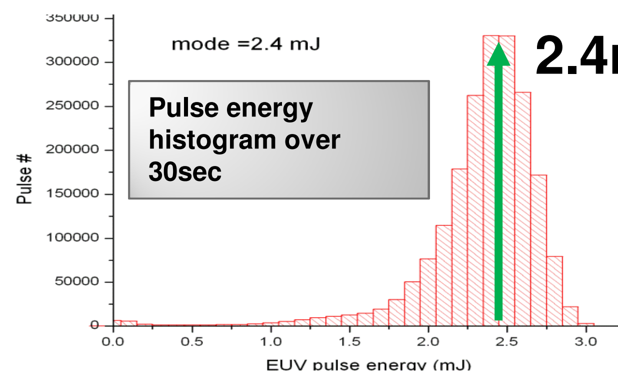
Roadmap to 250W EUV source power

Further pre-pulse development demonstrated Conversion Efficiency (CE) > 3%

High rep-rate laser with 10ns pulse duration

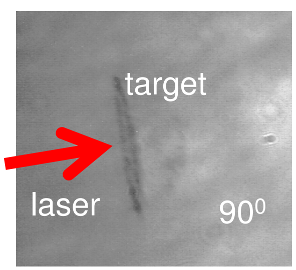


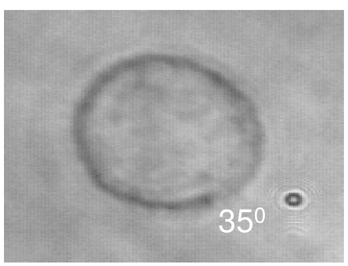
EUV:	2.4mJ
Rep rate:	60kHz
CO_2	18.3kW
EUV:	115W
CE:	3.1% - 3.4%



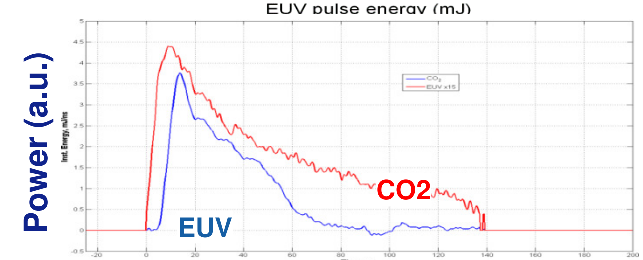
2.4mJ

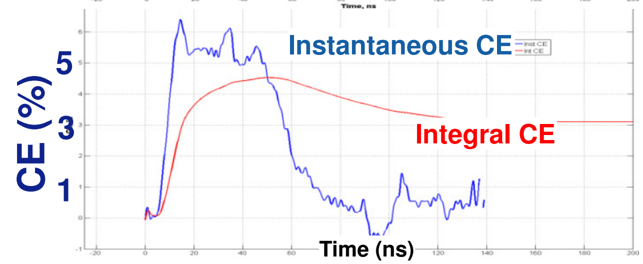
Low rep-rate laser with 150ps pulse duration





Instantaneous CE:	> 5%
Integral CE (max):	4.5%



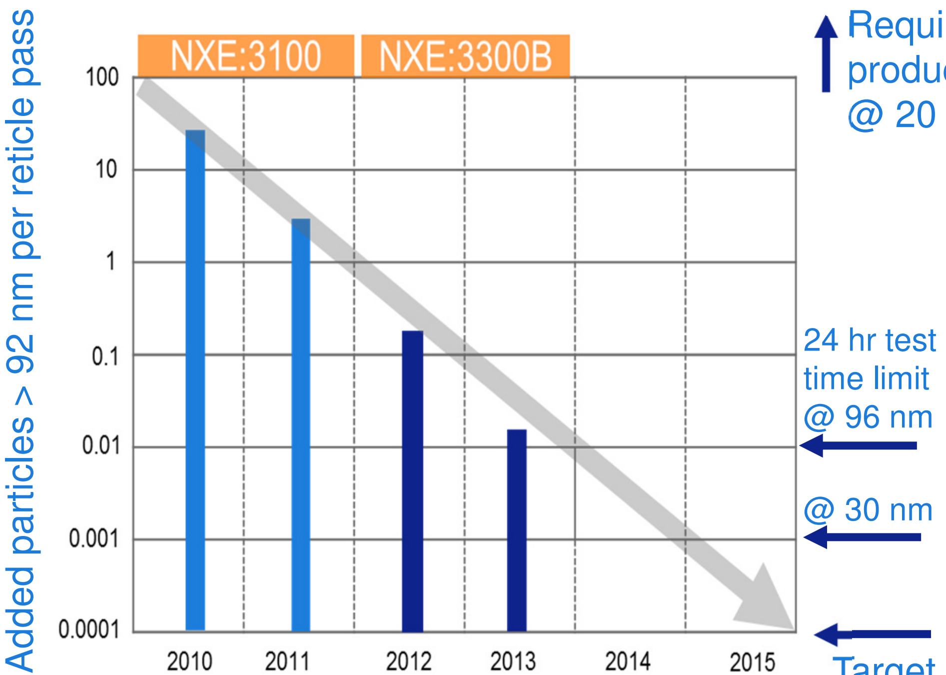


Presentation Outline

- Why EUV
- EUV roadmap, scanner & source status
- **EUV challenge**
  - Defectivity

The mask defect challenge

ASML achieved 10x per year improvement for pellicle-less operation (pellicle would reduce defect requirements substantially)

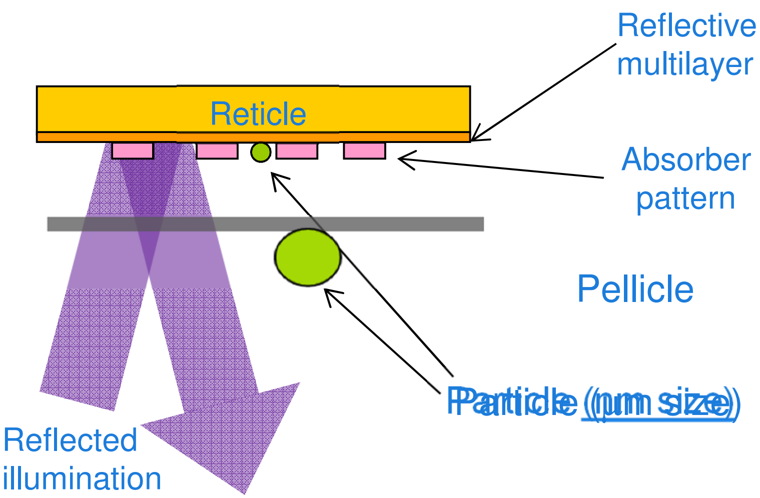


Progress made on ASML machines on added particles per reticle exchange over the past few years

Required for full production with pellicle @ 20 nm

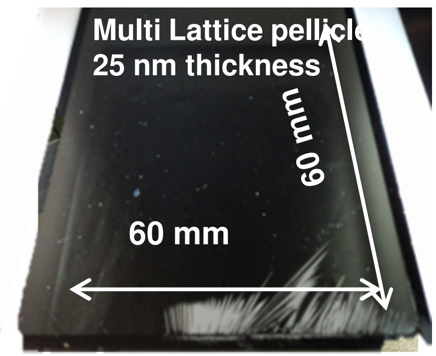
Target performance for full production without pellicle @ 20 nm

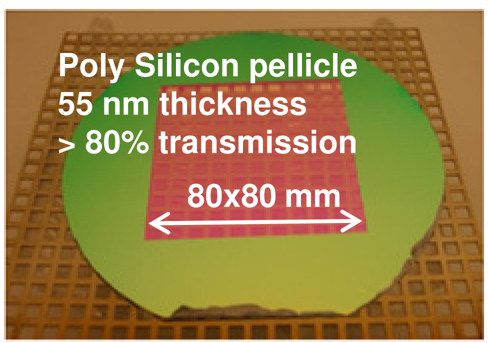
EUV Reticles (13.5nm)



The mask defect challenge

EUV pellicle considered as backup with minimum transmission and imaging loss

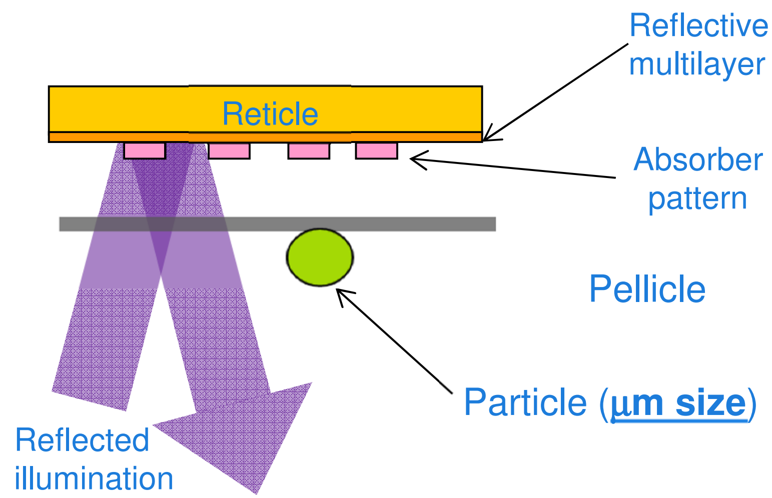




Wafer with **80*80 mm²** membrane

- Target full size
  - 110x144 mm²
- Transmission:
  - Required >90%
  - Achieved ~80%

EUV Reticles (13.5nm)



Conclusions

- EUV at > 70 WpH enables cost-effective shrink roadmap
  - Especially so for (random) 2D structures
- EUV maximizes Fab output and minimizes WIP and cycle time
- EUV performance meets customer requirements for 1x node
  - Roadmap for further performance improvement in place (Overlay, Imaging)
- EUV economics is gated by source power and collector lifetime roadmaps
  - Roadmap to 250W EUV source power in place
  - Collector cleanliness by debris mitigation and in-situ cleaning being targeted
- EUV mask defectivity improvement by 10x/year achieved over past years
  - Continuation of this trend targeted, pellicle developed as backup solution

Acknowledgements

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CATRENE
Cluster for Application and Technology Research in Europe on NanoElectronics

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